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NASA TECH BRIEF

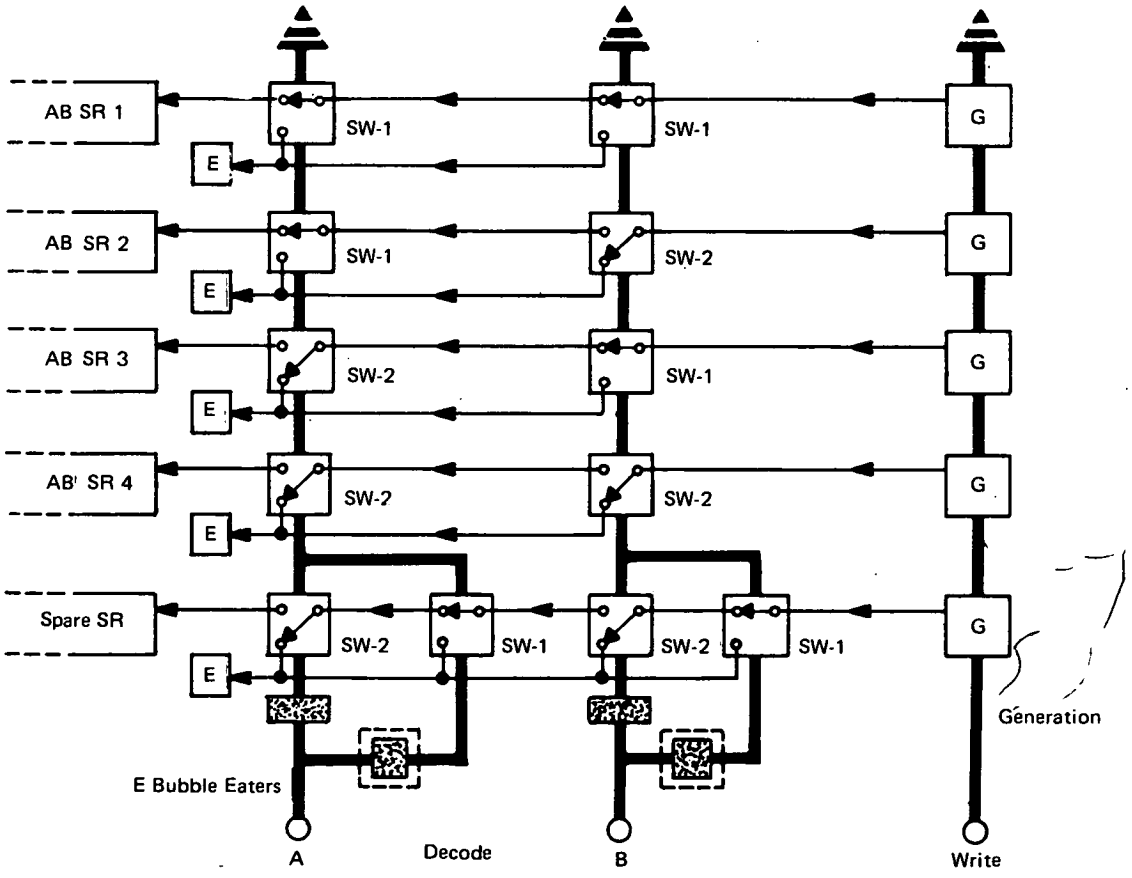
Marshall Space Flight Center

Redundancy Approaches in Bubble Domain Memories

The problem:

During the fabrication of integrated circuit chips, errors or inconsistencies appear which render portions of the elements of the chip useless.

The faulty chips must be discarded or each chip must contain a number of excess memory elements and interface connections so that the excess elements can be used in lieu of the faulty elements.



Alternate Areas To Be Selectively Etched After Testing

Redundancy Added To A Bubble Memory Chip

(continued overleaf)

The solution:

The makeup of each chip can be altered after fabrication to circumvent the faulty memory elements. This technique requires no additional interface connections and greatly reduces the number of excess or redundant elements formerly built into the chip.

How it's done:

A simplified block diagram of a bubble memory chip with redundancy is shown in the figure. Switch SW-1 is a "normally-upper-path" switch and SW-2 is "normally-lower-path".

The chip is tested after fabrication either electrically or visually. If all the regular shift registers, i.e., 1, 2, 3, and 4 in this case, perform correctly nothing more is done. The chip performs as a normal nonredundant chip with only four registers. No matter what combination of currents is applied to decode lines A and B, i.e., (++), (+−), (−+), or (−−), the magnetic bubble from the redundant generator always goes to a bubble eater.

If one of the four shift registers or its associated decoder section is faulty, the redundant register is given the personality of the faulty register as follows. In the decoder section corresponding to the spare register, each decode line branches out to two lines which then rejoin each other again. During the personalizing process one branch of line "A" and one branch of line "B" are opened Since the spare register can be switched in any one of four ways, the spare can be given the personality of any one of the four regular registers. The additional area per chip required for this capability is small because only the decoder is doubled in size. With a memory of 2^n shift registers of B bits each, the increase is:

$$\frac{(2n+\frac{B}{2})\quad 2^{-n}}{(n+\frac{B}{2})} + \frac{n}{(\frac{B}{2}+n)} \approx \frac{n}{(\frac{B}{2}+n)}$$

For example, a memory of 2^{16} shift registers (n=16) with 512 bits each (B=512), the increase in area is 1/17, of less than 10 percent. The line branches may be opened by selective etching, fusable links, or laser beams.

Notes:

1. Information concerning this innovation may be of interest to manufacturers of integrated circuitry.
2. Requests for further information may be directed to:
   Technology Utilization Officer
   Marshall Space Flight Center
   Code A&PS-TU
   Marshall Space Flight Center, Alabama 35812
   Reference: B72-10643

Patent status:

Inquiries concerning rights for the commercial use of this invention should be addressed to:

Patent Counsel
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